19.6 A Fully Reconfigurable Software-Defined Radio Transceiver in 0.13µm CMOS

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Since an energy-efficient digital software radio seems to remain a dream for a long time, the most practical solution for a multi-mode terminal (covering all cellular, WLAN, WPAN, broadcast, and positioning standards) is not just a reconfigurable RF front-end [1-3], but a true software-defined radio (SDR) that can be widely programmed to operate with all present and future standards. Numerous configuration "knobs" are added to a classical front-end, such that its performance and power can be tuned to any of the specific requirements of the envisioned standards to be covered. From the perspective of functionality, all its parameters (RF carrier frequency, channel bandwidth, noise figure, linearity, filter characteristic, etc.) should be reconfigurable over a very wide range. But there is an equally important perspective of energy optimization that allows the front-end to use the same reconfiguration knobs to reduce its power consumption in a particular mode when allowed by the conditions of the environment, e.g., reduce the filtering attenuation level when the interferer level is lower than the worst case defined by the standard. This enables the reconfigurable front-end to fulfill the specifications of each standard, thus implementing an SDR at a power similar to a single-mode radio that at the same time operates at significantly lower average power consumption due to real-time power/performance trade-offs [4].

A conceptual view of the presented SDR transceiver front-end is shown in Fig. 19.6.1. The active core, implemented in a plain 0.13µm CMOS process, includes a fully reconfigurable direct-conversion receiver, transmitter, and two synthesizers (for FDD operation). The direct-conversion scheme is used since it can be reconfigured over a broad range. The performance of each block in the proposed SDR device can be digitally adjusted over a wide range of specifications.

A key aspect for the RF part is its interference robustness. The blocking requirements for simultaneous multi-mode operation imply the need for tunable narrow-band circuits at the antenna interface. In this work, the option of using MEMS switches to build a low-loss reconfigurable antenna filter section on a thin-film substrate is explored. This is the case for the LNA, whose active CMOS part is co-designed with the MEMS switch as well as the passive off-chip matching. The circuit schematic of Fig. 19.6.2 [5] shows that multi-band operation is achieved independent of the inductive emitter degeneration. A single-pole dual-throw (SPDT) MEMS switch is used to connect the LNA to either its 1.8GHz matching circuit and antenna filter, or to its 5GHz section which uses just the bonding wire for input matching. To prove this concept with a commercial component, a packaged MEMS switch [6] is mounted on a PCB together with the CMOS die. This device has limited the validation of the proposed system to only 2 bands. Performance is only slightly affected since the loss of the switch including its package is measured to be only 0.2dB. A mature technology that integrates MEMS switches in an MCM technology [7] will make it feasible to build more complex structures covering a broad range of frequency bands.

Internally, the LNA has an LC-tuned output branch for the high band, and a resistively loaded branch for frequencies lower than 2.5GHz. A shunt cascode branch provides gain switching. Both outputs pass through a multiplexing single-ended-to-differential converter towards the direct-downconversion mixer, which has a current-mode output with a 7b programmable gain. In the baseband, channel filtering is provided by an active-G_m-RC low-pass filter [8] that can independently set its order (with a 2nd-, 4th-, or 6th-order transfer function), its channel bandwidth (continuously programmable between 350kHz and 23MHz), and its input-referred noise level by controlling the R- and C-values. The variable-gain amplifier can in a similar way not only program its gain but also its bandwidth and noise level. All control is not based on just setting e.g., the cutoff frequency to a predetermined value, but instead it is based on optimizing the overall quality of the received signal.

Two fractional-N synthesizers (Fig. 19.6.3) are integrated on chip for FDD carrier generation. Each one contains a wide-tuning range VCO with switchable active core and sensitivity [9], as well as a programmable charge pump and loop filter. A fully flexible VCO distribution network routes the 3 to 5GHz signal of each PLL (or of an external source) to the receiver, the transmitter, and/or the external world. This external interface is used for MIMO operation, where multiple transceiver ICs share a common LO signal, generated by one of them. The VCO signal is processed by the divide-multiply-quadrature (DMQ) block to drive the mixers. This DMQ circuit generates quadrature LO signals in the whole band from 6GHz down to 150MHz, with the constraint that the VCO never runs at the RF frequency to avoid the well-known coupling problem in direct-conversion radios. The first block of the DMQ is a programmable frequency divider with a modulus ranging from 2 to 20. Since division by an odd number cannot generate quadrature signals, a duty-cycle correction (DCC) block is included. Quadrature LO signals higher than 2.5GHz cannot be generated by simple division, so the divider output is multiplied again by means of a 90° DLL [10] to provide signals up to 6GHz.

For transmission, a direct-upconversion architecture uses a similar reconfigurable low-pass filter, Gilbert mixers, and a wideband output driver. The full device programmability with a huge amount of bits to control the settings of each building block is managed by a scalable network-on-chip (NoC) that controls each circuit based on the input data it gets from a serial interface.

Figure 19.6.7 shows the micrograph of the IC ($3.0\times3.8mm^2$) and its implementation on PCB together with the MEMS switch. A receive budget measurement is shown in Fig. 19.6.4 for 3 different channel bandwidths. The SNDR is limited by thermal noise for low input powers (total RX chain minimum NF=4dB including PCB). The 1/f noise corner is around 200kHz, which explains the higher NF for the low-BW mode. Realistic interferer and blocker levels are used, corresponding to a Bluetooth, UMTS, and WLAN scenario, respectively. This causes the front-end to reduce its LNA gain at higher input power levels with sometimes a resulting small dip in the SNR. At high input powers distortion is the limit (IIP3 = –9dBm). A typical TX output spectrum with 64QAM OFDM modulation is shown in Fig. 19.6.5. The PA/PPA is not integrated in this prototype, the last stage uses only 5mA so P_{1dB} is –15dBm. An excellent constellation diagram is transmitted, EVM equals 2.2% and ACPR is –42dB.

Figure 19.6.6 summarizes the measured performance of the SDR transceiver. Depending on the specific system requirements in each mode, all building blocks are appropriately configured through the NoC and performance can be controlled widely. Although only the extreme cases are listed, all intermediate settings are also available. The very wide reconfiguration range achieved without compromising actual performance shows that this prototype has taken an important step towards a true energy-efficient multi-mode SDR.

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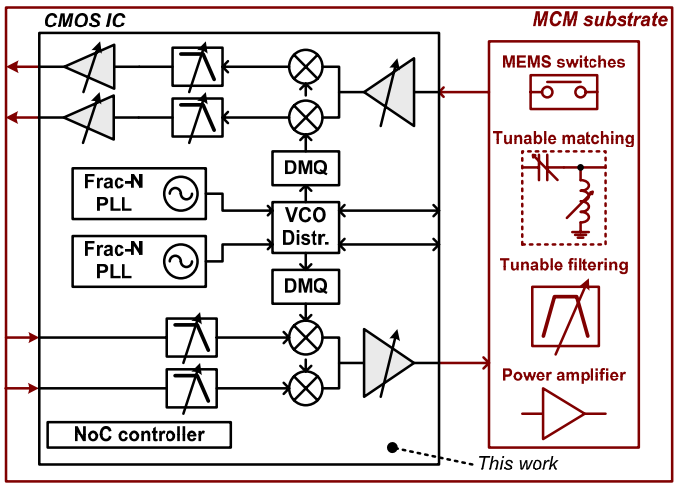

Figure 19.6.1: Conceptual view of the SDR transceiver front-end.

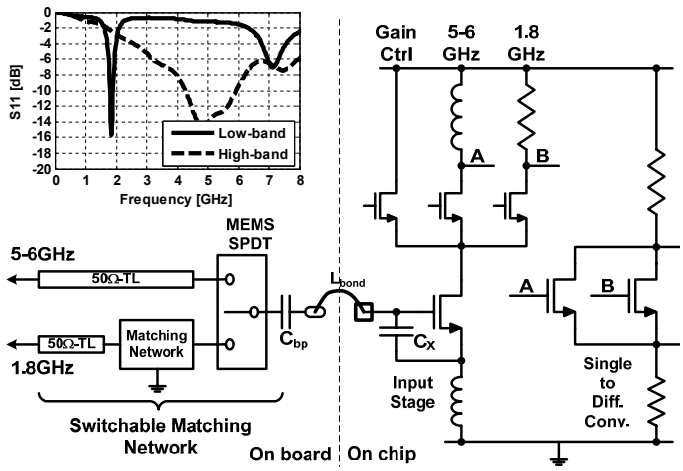

Figure 19.6.2: CMOS/MEMS co-designed dual-band LNA circuit schematic and input-matching measurement (inset).

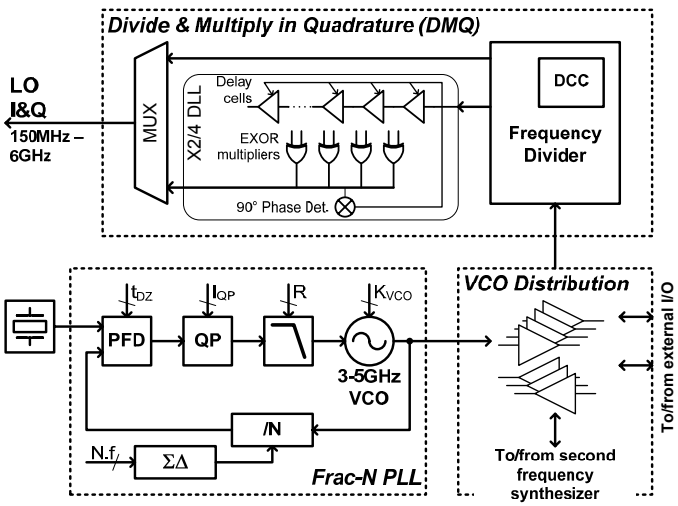

Figure 19.6.3: Multiple-decade frequency synthesizer block diagram.

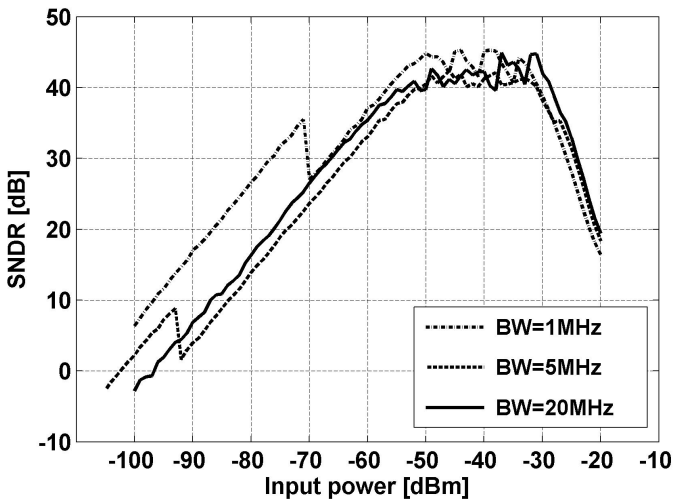

Figure 19.6.4: RX chain radio budget measurement.

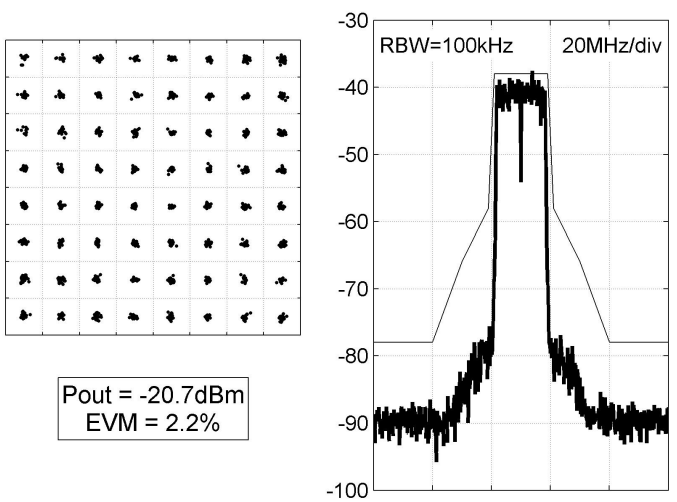

Figure 19.6.5: TX 64QAM constellation diagram and output spectrum.

Power supply = 1.2V				
Current consumption	[mA]	(min/typ/max)		[mA]
Receiver LNA	7/10/12	**Transmitter** PPA		10
Mixer	2 × 5/9/12	Mixer		2 × 6
LO buffer	2 × 3/4/7	LO buffer		2 × 3/4/7
LPF (10MHz, low noise)	2 × 10	LPF (10MHz)		2 × 4
(500kHz, high noise)	2 × 0.3	(1MHz)		2 × 0.3
VGA (low noise, high BW)	2 × 6			
(high noise, low BW)	2 × 1	**LO DIST**		8
		DMQ	/3, ×4 5GHz	23
PLL VCO	4/7/10		/3, ×2 2.5GHz	20
Divider	3		/2 2GHz	6
PFD, QP, LPF	3		/4 1GHz	7

Receiver performance		**Transmitter performance**	
NF	4 .. 8 dB	P1dB	−13 to −17dBm
Gain	10 .. 90dB	OIP3	−1 to −5dBm
IIP3	-9dBm		
Center freq.	1.8 & 5 to 6GHz*	Center freq.	150MHz to 6GHz*
Channel BW	350kHz to 23MHz	Channel BW	1 to 16MHz
Current	62 to 120mA	Current	56 to 89mA

*a bug in the DLL prevents RX and TX measurements above 2.5GHz

Figure 19.6.6: Performance overview.

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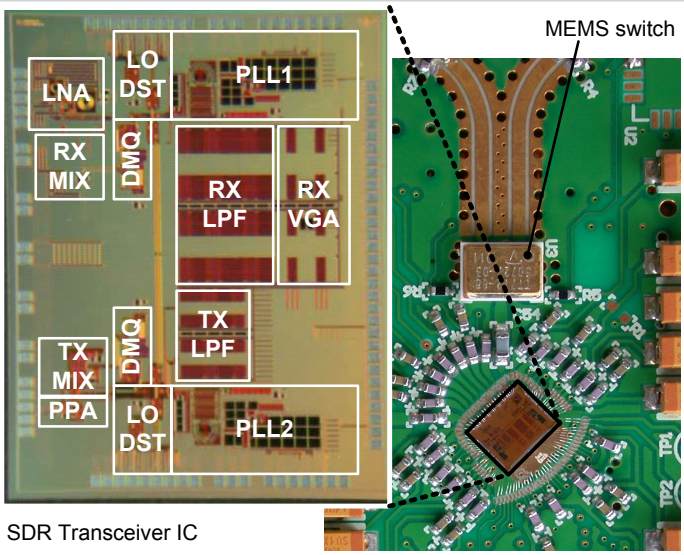

Figure 19.6.7: Die micrograph and MEMS PCB.

